Obtaining asynchronous benefits from synchronous design flow

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1. Introduction

Asynchronous logic has for a long time shown many benefits but has largely been ignored by industry due to the maturity of the design methodologies. The implementation methods of asynchronous circuits take time to learn, take longer to design and verifying them is very difficult. Companies are not interested in design methods which require their entire work force to be retrained.

This paper introduces a direct translation is a system which allows synchronous designs generated from tools such as VHDL, Verilog or schematics to be automatically converted to asynchronous counterparts. All functional testing of the design can be done on the original synchronous version to allow minimal exposure to the asynchronous circuit.

2. Direct translation

Direct translation requires minimal user interaction. A translation table, which describes the asynchronous counterparts to synchronous components and structures, is used to replace all elements of the synchronous design with asynchronous elements. The design would then be a fully functional asynchronous circuit. Not only do synchronous elements need to be replaced with asynchronous counterparts but structures such as wire forks also need to be detected and replaced.

An optimizing pass can improve performance and reduce area by combining C-elements together. This can be tuned to either optimise for area or for speed. If the speed option is chosen then some C-elements may be duplicated. This can improve speed but increases the area.

2.1. Technology mapping

The generated asynchronous circuit can be mapped onto one of a number of technologies. Dual-rail DIMS is the simplest target due to its QDI property. Although QDI circuits do place assumptions on the delay of wire forks, these are easily met.

DIMS is a safe target but the circuit performance is very poor. Other target technologies give better performance and lower area. Ongoing work is taking place creating other technologies.

2.2. Optimization

Although the translator will produce functionally correct circuits extra elements need to be placed in the design to match the performance of the synchronous design. The most common of these performance-boosting elements is the pipeline latch. To place a pipeline latch into the design, an element behaving as a buffer is added to the synchronous design. This element is recognised during the conversion and is replaced with a pipeline latch in the asynchronous circuit. This allows elements to be placed in the asynchronous design without having an adverse effect on the synchronous version.

2.3. Microprocessor example

A direct translation technique was used to convert a ready-made synchronous 32bit microprocessor. Only a few hours of effort for adding pipeline latches was required to convert the design into a fast asynchronous version. The final circuit shows a performance increase of about 10% to 30% against the original synchronous design. Even better results could be gained by spending more time on the placement of other performance enhancing elements.

3. Conclusion

Direct translation is a very easily adoptable technique allowing both fast implementation time and full control of the output circuit. It allows fault free re-implementation of old synchronous designs and new designs can be easily made using existing familiar synchronous tools.

Exposure to asynchronous design is kept to the minimum. All functional testing is done on the synchronous version. QDI technologies such as dual-rail DIMS generate robust implementations minimising the need for post-layout simulations. All of the design is conducted using standard synchronous tools including the optimisations in the asynchronous design.